LH53V8000

CMOS 8M (1M × 8 / 512K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- 1,048,576 words × 8 bit organization
  (Byte mode)
  524,288 words × 16 bit organization
  (Word mode)
- Access times:
  200 ns (MAX.) at 3.0 V ≤ V_{CC} < 4.5 V
  100 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Power consumption:
  Operating:
  550 mW (MAX.)
  4.5 V ≤ V_{CC} ≤ 5.5 V
  315 mW (MAX.)
  3.6 V < V_{CC} < 4.5 V
  126 mW (MAX.)
  3.0 V ≤ V_{CC} ≤ 3.6 V
  Standby: 550 µW (MAX.)
- Static operation
- Three-state outputs
- Wide range power supply: 3.0 V to 5.5 V
- Mask-programmable $OE_1/\overline{OE_1}$/DC
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH53V8000 is an 8M-bit mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

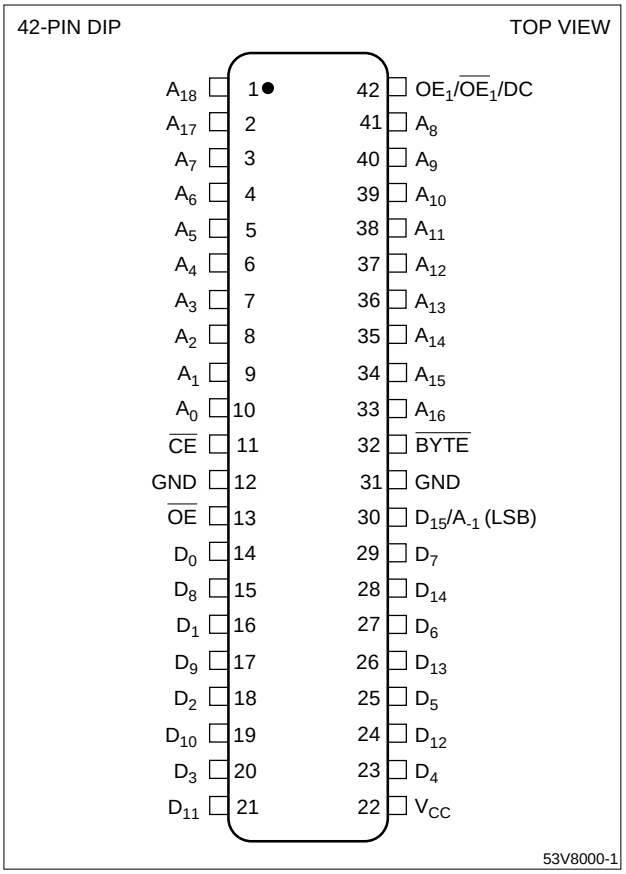


Figure 1. Pin Connections for DIP Package

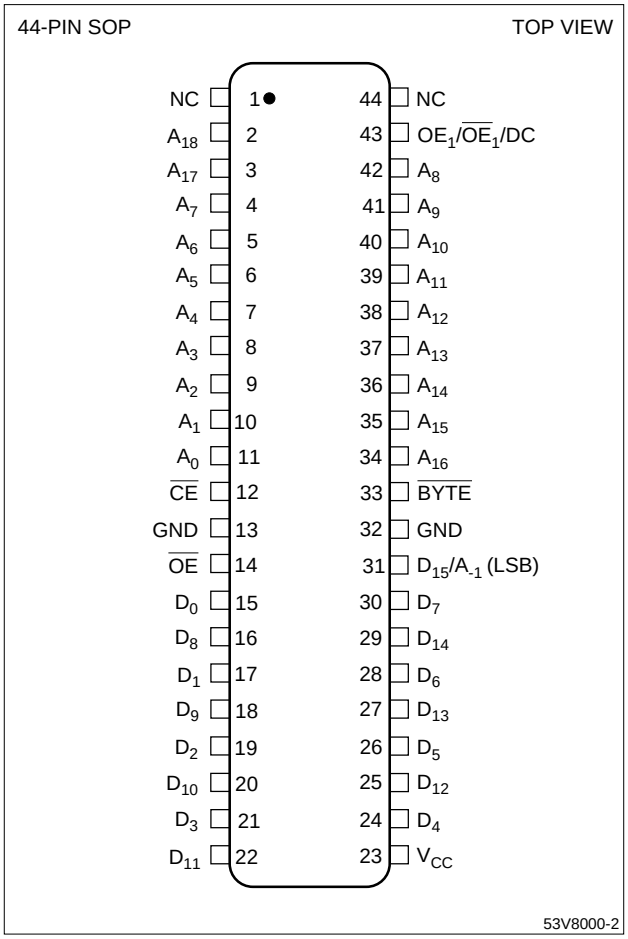


Figure 2. Pin Connections for SOP Package

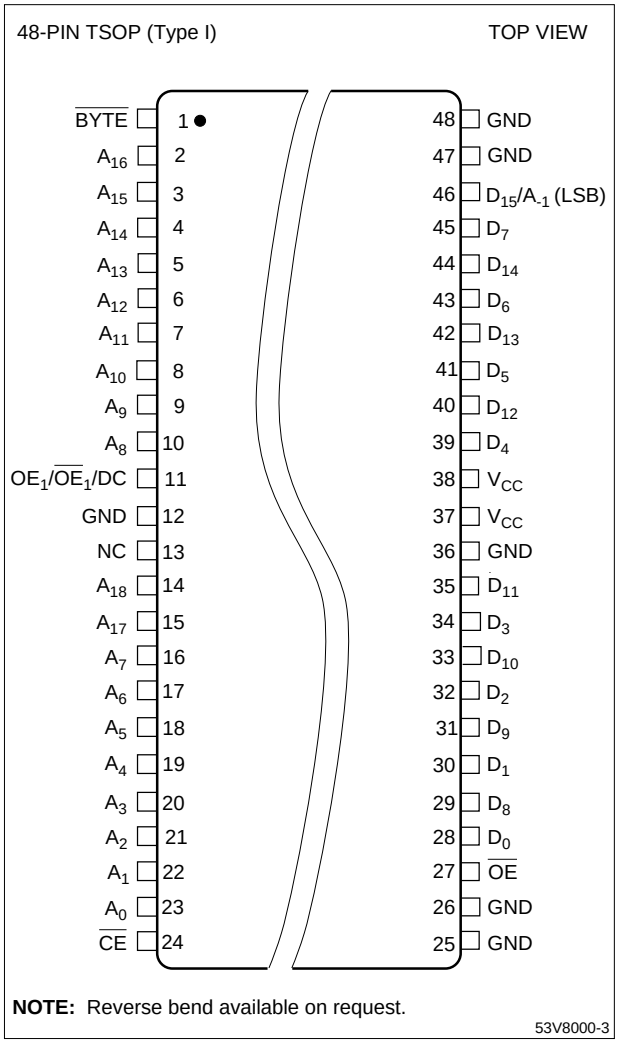


Figure 3. Pin Connections for TSOP (Type I) Package

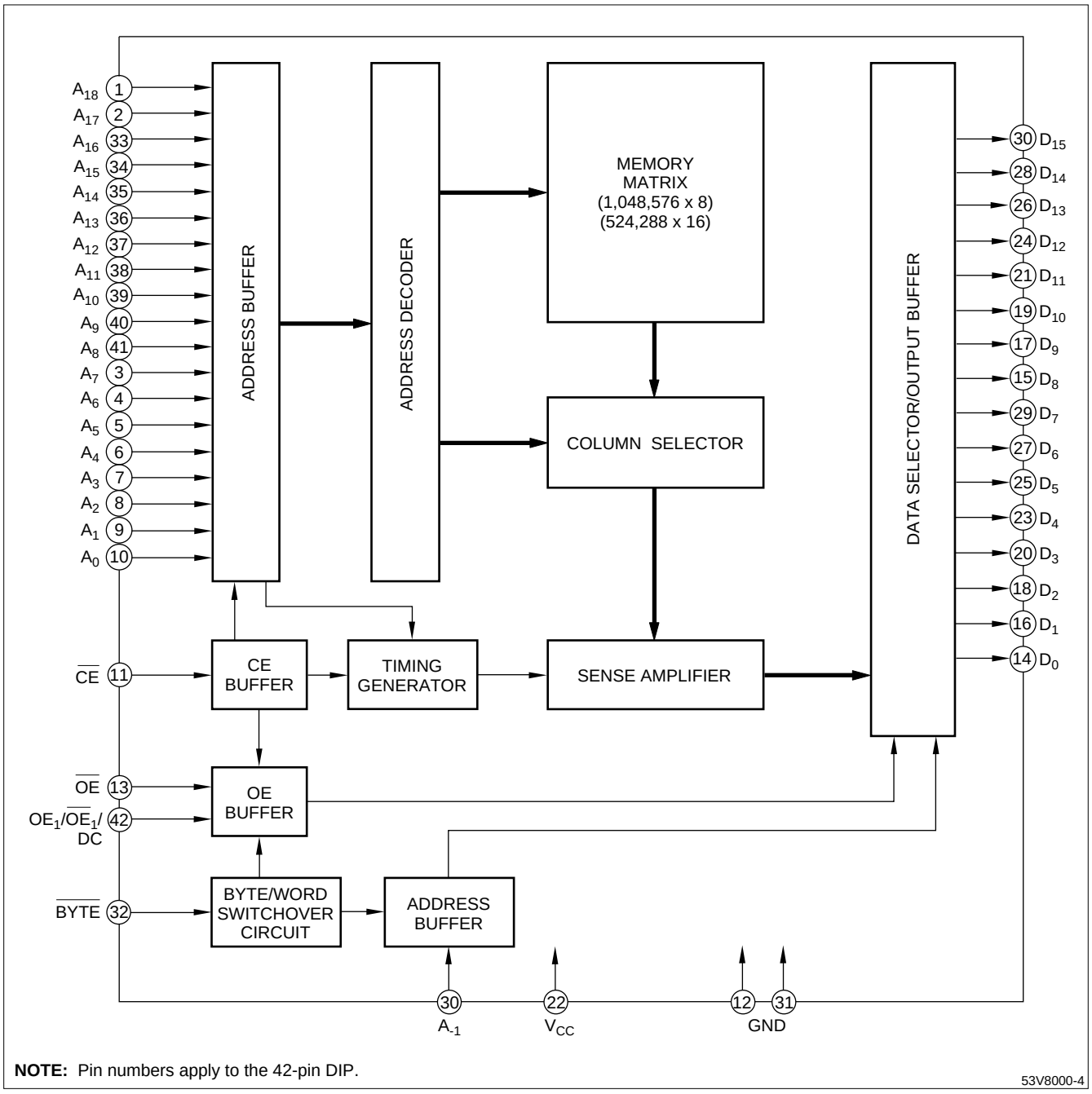


Figure 4. LH53V8000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
$A_{-1} – A_{18}$	Address input	1
$D_0 – D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output enable input	
$OE_1/\overline{OE_1}$/DC	Output enable input	2, 3
V_{CC}	Power supply	
GND	Ground	

NOTES:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.
2. Active levels of $OE_1/\overline{OE_1}$/DC are mask-programmable. When DC is selected out of $OE_1/\overline{OE_1}$/DC, it is fixed to an active level. Then it is recommended to apply either 'HIGH' or 'LOW' level to the DC pin.
3. DC = Don't Care.

TRUTH TABLE

$\overline{CE}$	$OE_1/\overline{OE}$, $\overline{OE_1}/$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
				$D_0 – D_7$	$D_8 – D_{15}$	LSB	MSB	
H	X	X	X	High-Z	High-Z	–	–	Standby
L	L/H	X	X	High-Z	High-Z	–	–	Operating
L	H/L	H	Input inhibit	$D_0 – D_7$	$D_8 – D_{15}$	A_0	A_{18}	Operating
L	H/L	L	L	$D_0 – D_7$	High-Z	A_{-1}	A_{18}	Operating
L	H/L	L	H	$D_8 – D_{15}$	High-Z	A_{-1}	A_{18}	Operating

NOTE:
X = H or L.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	3.0		5.5	V

DC CHARACTERISTICS (V_{CC} = 3.0 to 5.5 V, T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'Low' voltage	V_{IL}		–0.3	0.4	V	
Input 'High' voltage	V_{IH}		0.8 × V_{CC}	V_{CC} + 0.3	V	
Output 'Low' voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –400 µA	0.8 × V_{CC}		V	
Input leakage current	| I_{LI} |	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	| I_{LO} |	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns		100	mA	2
	I_{CC2}	t_{RC} = 200 ns		70	mA	3
	I_{CC3}	t_{RC} = 200 ns		35	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, T_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH}, OE_1 = V_{IL}
2. 4.5 ≤ V_{CC} ≤ 5.5 V, outputs open
3. 3.6 < V_{CC} < 4.5 V, outputs open
4. 3.0 ≤ V_{CC} ≤ 3.6 V, outputs open

AC CHARACTERISTICS (T_A = 0°C to +70°C)

PARAMETER	SYMBOL	3.0 ≤ V_{CC} < 4.5		4.5 ≤ V_{CC} ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	200		100		ns	
Address access time	t_{AA}		200		100	ns	
Chip enable access time	t_{ACE}		200		100	ns	
Output enable delay time	t_{OE}		100		50	ns	
Output hold time	t_{OH}	10		5		ns	
CE to output in High-Z	t_{CHZ}		100		40	ns	1
OE to output in High-Z	t_{OHZ}						

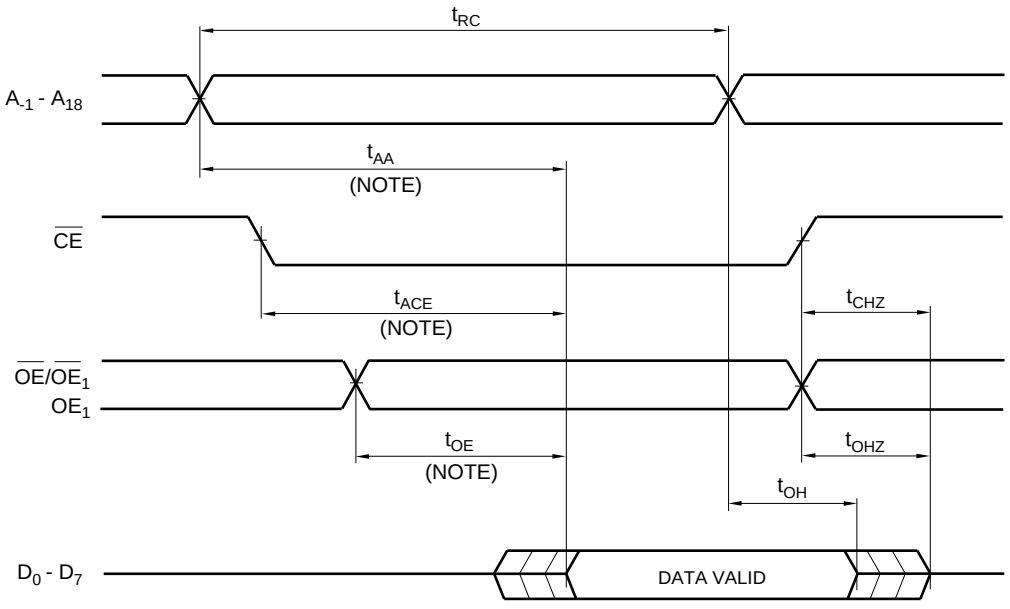
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 V to (0.8 × V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	(V_{CC}/2) V
Output load condition	1TTL + 100 pF

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.



NOTE: The output data becomes valid when the intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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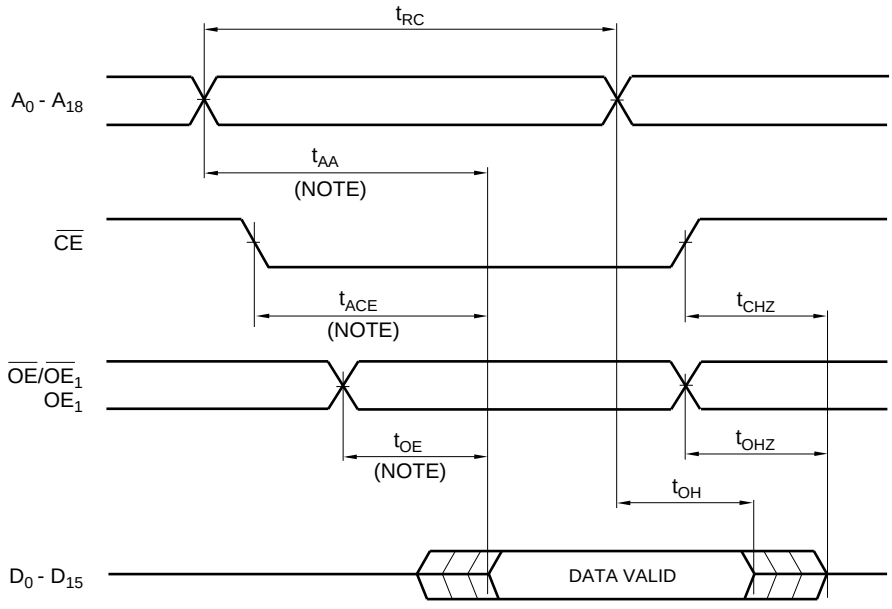
Figure 5. Byte Mode ($\overline{BYTE}$ = V_{IL})



NOTE: The output data becomes valid when the last intervals, t_{AA}, t_{ACE}, or t_{OE}, have concluded.

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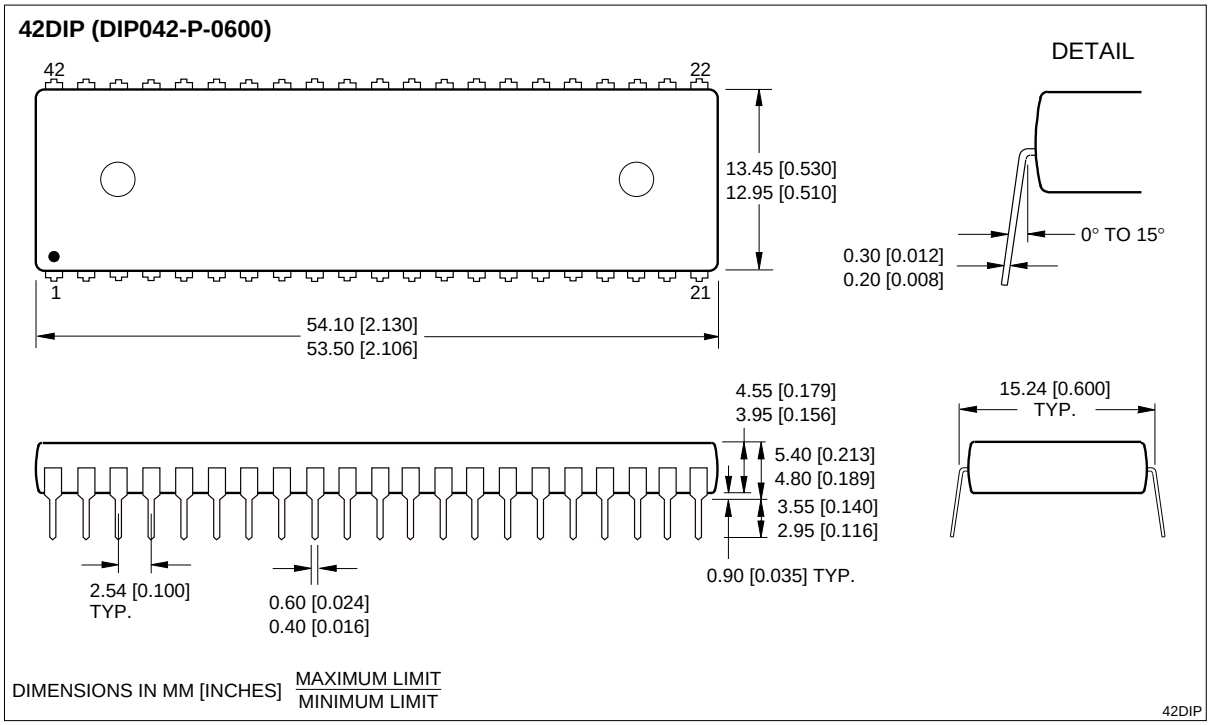
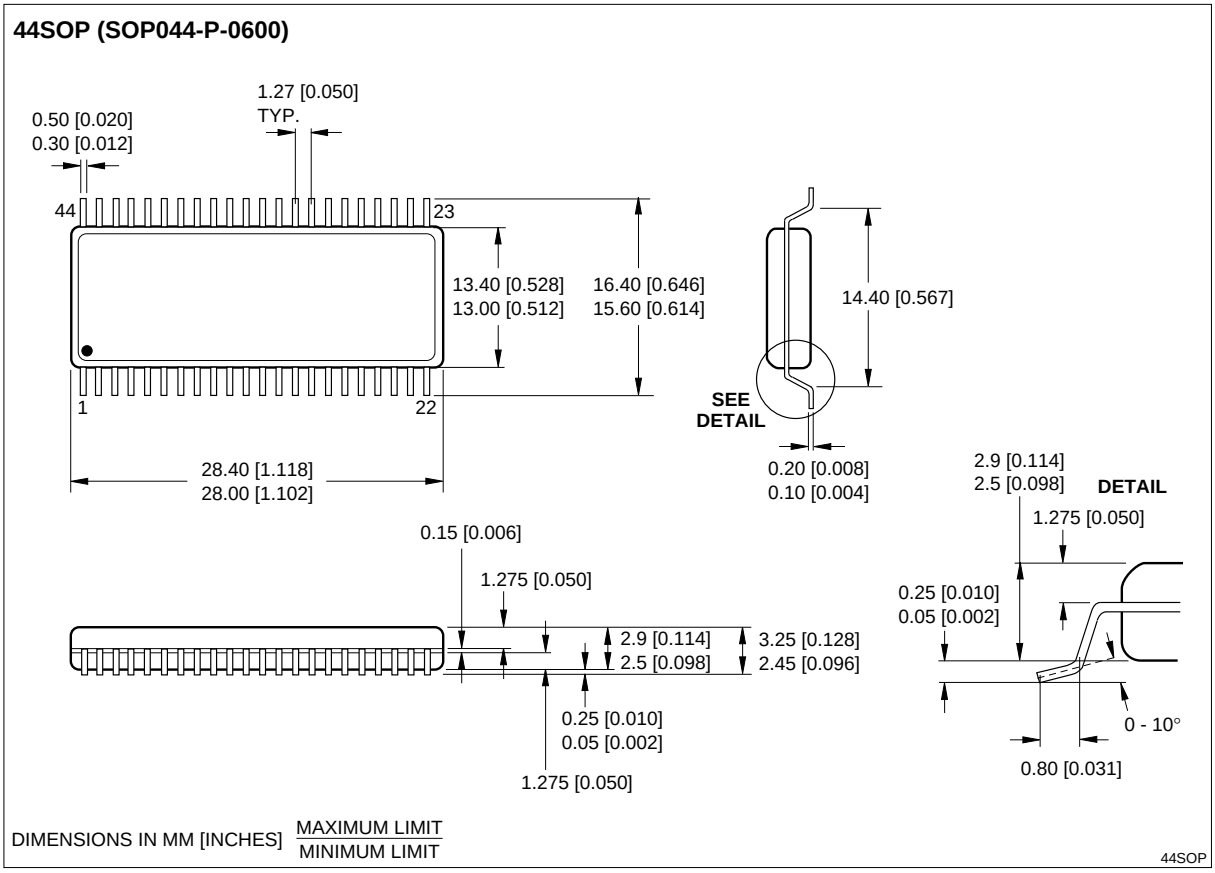
Figure 6. Word Mode ($\overline{BYTE}$ = V_{IH})

PACKAGE DIAGRAMS

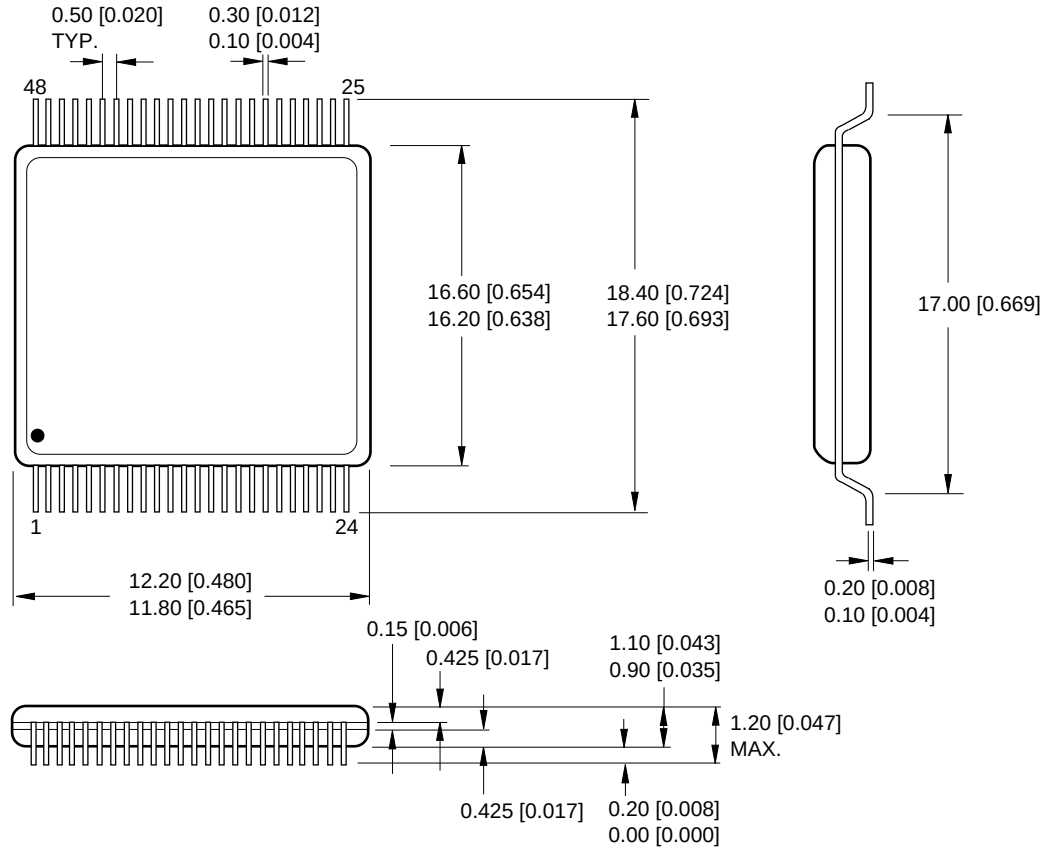


42-pin, 600-mil DIP



44-pin, 600-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH53V8000 — Device Type
X — Package

- D 42-pin, 600-mil DIP (DIP042-P-0600)
- N 44-pin, 600-mil SOP (SOP044-P-0600)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

- CMOS 8M (1M x 8 or 512K x 16) Mask-Programmable ROM, Low-Voltage Operation

Example: LH53V8000D (CMOS 8M (1M x 8 or 512K x 16) Mask-Programmable ROM, Low-Voltage Operation, 42-pin, 600-mil DIP)

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